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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, May 2014
(2008 Scheme)
Branch : ELECTRONICS AND COMMUNICATION ENGINEERING
08.405 : Analog Integrated Circuits (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Define slew rate. What causes the slew rate ?
2. Draw the circuit diagram of a practical Wien bridge oscillator with adaptive negative feedback.
3. List three open loop opamp configurations. Explain why open loop opamp configurations are not used in linear applications.
4. Design an opamp circuit to obtain $V_0 = -2V_1 + 3V_2 + 4V_3$. Use minimum value of resistance as 10 kΩ .
5. Design a 50 Hz Notch filter. Draw the circuit.
6. Draw and explain a switched capacitor resistor.
7. Calculate the values of the LSB, MSB and full scale output for an 8 bit DAC for the 0 to 10V range.
8. Explain the block diagram of a PLL. Suggest two applications of PLL.
9. Draw and explain the functional block diagram of a 723 regulator IC.
10. Draw the basic 8038 connection for fixed frequency and 50% duty cycle operation. Write the expression for f_0.

P.T.O.

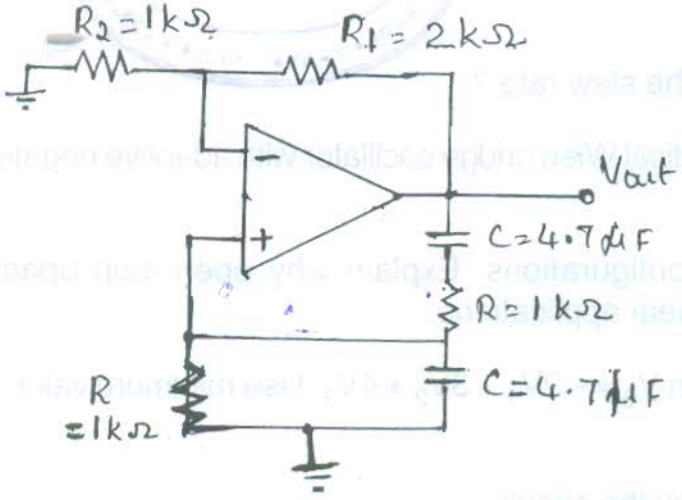
PART – B

Answer **any two** questions from **each** Module.

Module – I

11. Explain the significance of frequency compensation in opamp. How is frequency compensation done in a two stage opamp ? 10

12. Determine the frequency of the oscillations of the circuit shown. Assume the opamp to be ideal. 10



13. a) Draw the circuit of a monostable multivibrator using opamp. Explain its operation. 5

    b) What are the different types of voltage to current converters ? Explain any one. 5

Module – II

14. Design a sallen key second order low pass filter with f_0 = 1kHz and Q = 2. 10

15. Draw the circuit of a first order switched capacitor low pass filter. Explain its operation. What are the limitations of switched capacitor filters ? 10

16. a) Draw the circuit of a 4-bit R-2R ladder network based DAC and explain its working. 6

    b) The basic step of a 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output is produced if the input is 101100101. 4

Module – III

17. a) Design a monostable multivibrator using 555 timer to produce a pulse width of 100 ms. 5

    b) Draw and explain emitter coupled VCO. 5

18. a) Design a current limit circuit for a 723 regulator to limit the current to 60 mA. 6

    b) Explain how current boosting is done in IC 723. 4

19. Derive the expressions for lock-in range and capture range of IC 565. 10